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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,145	WADA, SHIGEKI	
	Examiner	Art Unit	
	ADOLF DSOUZA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's changes to the Abstract have been accepted by the Examiner.

2. Applicant's response to the claim objections made have been accepted by the Examiner.

3. Applicant's arguments filed 9/25/2009 have been fully considered but they are not persuasive.

Argument: Applicant argued that " The Examiner has identified sub-portions of the phase-locked loop circuit shown in Figure 7 of Miyashita et al. as corresponding to particular claim elements, without regard to the context in which these circuit elements are disclosed in the Miyashita et al. reference and without citing any teaching which would have led one skilled in the art to combine the elements to produce the claimed clock and data recovery circuit. In particular, the elements ... " (Remarks 9/25/2009, page 10, last paragraph – page 11, 1st paragraph in particular and also related Argument on pages 11 - 13).

Response: Examiner respectfully disagrees. As stated in the last Office Action, Miyashita discloses in Fig. 7, the discriminator circuit, phase detector and the clock signal. These are clearly shown in Fig. 7, within the box labeled 20 as a single unit. One of ordinary skill in the art can easily combine that single unit with what is disclosed in AAPA to arrive at Applicant's invention. If the pieces are not disclosed as 3 separate entities, then one could argue that the Examiner was taking a piecemeal approach. However that is not the case. Therefore, Examiner disagrees with Applicant's argument that Miyashita does not disclose all the claim limitations and that there is no motivation

to combine unit 20 in Applicant's AAPA. The motivation and benefits to use such a unit in Applicant's AAPA is clearly described by Miyashita (column 2, lines 30 – 50).

In view of the above, Examiner, is maintaining his rejection as in the last Office Action.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12 – 16, 24 - 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter AAPA) in view of Miyashita et al (US 5610954).

Regarding claim 12, AAPA discloses a clock and data recovery circuit (Applicant's Fig. 11) comprising:

a phase synchronization loop including an oscillator, the oscillation frequency of which is variably controlled, said phase synchronization loop performing phase-synchronization of a clock signal output from said oscillator with an input data signal

(Fig. 11; Specification [0021]; wherein the phase synchronization loop is formed by elements 902, low pass filter, oscillator 909; the oscillation frequency being controlled by the output of the loop filter and the phase detector receives as inputs the Data input signal and VCO output);

and a phase shift circuit for shifting the phase of the clock signal, output from said oscillator, based on a comparison result output from said phase detector circuit (Fig. 11, variable delay element 912; wherein element 912 phase shifts the output of the VCO 909);

AAPA does not disclose a discriminator circuit that has the data signal as its input.

In the same field of endeavor, however, Miyashita discloses a discriminator circuit, responsive to a clock signal for discrimination, for discriminating said input data signal and outputting the discriminated signal (Fig. 7, elements 21A and 22A; wherein element 21A, 21B are interpreted as the discriminator circuit and element 22A does the phase comparison between the input signal and the discriminator output);

a phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said input data signal (Fig. 7, element 22A; wherein element 22A does the phase comparison between the input signal and the discriminator output);

the clock signal, output from said phase shift circuit, being supplied as said clock signal for discrimination to said discriminator circuit (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the phase discriminator, as taught by Miyashita, in the system of AAPA because this would for allow for the output data to be locked to the input data signal.

Regarding claim 13, AAPA discloses a clock and data recovery circuit (Applicant's Fig. 11) comprising:

a first feedback loop at least including a first phase detector circuit for detecting the phase difference between a clock signal and a received data signal (Fig. 11; Specification [0021]; wherein the 1st feedback loop is formed by elements 902, low pass filter, oscillator 909; the oscillation frequency being controlled by the output of the loop filter and the phase detector receives as inputs the Data input signal and VCO output);

a second feedback loop and a second phase detector circuit for detecting the phase difference between the data signal, discriminated and output by said discriminator circuit, and said received data signal (Fig. 11, elements formed by 910, low pass filter, 912);

and a clock recovery circuit for being controlled by said first and second feedback loops to output the clock signal recovered (Fig. 11, 1st and 2nd loops giving output "Clock Out");

AAPA does not disclose a discriminator circuit that has the data signal as its input.

In the same field of endeavor, however, Miyashita discloses a discriminator circuit supplied with said received data signal (Fig. 7, elements 21A and 22A; wherein element 21A, 21B are interpreted as the discriminator circuit and element 22A does the phase comparison between the input signal and the discriminator output) and the clock signal output from said clock recovery circuit being supplied as a clock signal for discrimination by said discriminator circuit (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the phase discriminator, as taught by Miyashita, in the system of AAPA because this would for allow for the output data to be locked to the input data signal.

Regarding claim 14, AAPA discloses the first feedback loop includes:

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage (Fig. 11, element 909 which receives control voltage from the loop filter output);

a first phase detector circuit supplied with a clock signal output from said voltage-controlled oscillator circuit and with said received data signal to detect the phase difference between the two input signals (Fig. 11, element 902);

and a first integrator circuit for integrating an output of said first phase detector circuit and for supplying an output voltage to said voltage-controlled oscillator circuit as a control signal voltage (Fig. 11, element low pass filter in upper path);

and wherein said second feedback loop includes:

a second integrator circuit for integrating an output of said second phase detector circuit (Fig. 11,element low pass filter in lower feedback loop);

and a phase shift circuit receiving said clock signal output from said voltage-controlled oscillator circuit and an integrated output of said second integrator circuit, for shifting the phase of said clock signal in accordance with the integrated output received, to output the resulting clock signal (Fig.11, element variable delay that does the phase shifting);

AAPA does not disclose a discriminator circuit that has the data signal as its input.

In the same field of endeavor, however, Miyashita discloses a discriminator circuit supplied with said received data signal (Fig. 7, elements 21A and 22A; wherein element 21A, 21B are interpreted as the discriminator circuit and element 22A does the phase comparison between the input signal and the discriminator output);

a second phase detector circuit supplied with an output data signal, output from said discriminator circuit, and with said received data signal, to detect the phase difference between the two signals supplied (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B);

said clock signal, output from said phase shift circuit, being supplied to said discriminator circuit as a clock for discrimination and output as an output clock signal (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the phase discriminator, as taught by Miyashita, in the system of AAPA because this would for allow for the output data to be locked to the input data signal.

Regarding claim 26, AAPA discloses first phase detector circuit compares the phase of said received data signal supplied to a first input end thereof with that of said clock signal supplied to a second input end thereof to output a comparison result at an output end thereof (Fig. 11, element 902);

said first integrator circuit is supplied with an output signal from said first phase detector circuit to integrate the signal supplied (Fig. 11, element low pass filter in upper path);

said clock recovery circuit includes a voltage-controlled oscillator supplied with an output signal of said first integrator circuit at an input end thereof to change the oscillation frequency based on an output signal from said first integrator circuit to output the resulting clock signal at an output end thereof (Fig. 11, element 909);

said clock signal, output from said clock recovery circuit, being fed back to a second input end of said first phase detector circuit (Fig. 11, element VCo output going to phase detector 912 input);

said second integrator circuit is supplied with an output signal from said second phase detector circuit to integrate the signal supplied (Fig. 11, element pow pass filter in lower feedback loop);

and a phase shift circuit supplied with said clock signal output from said clock recovery circuit at an input end thereof and with an output signal from said second integrator circuit at a control signal input end thereof to shift the phase of the clock signal output from said clock recovery circuit, based on said output signal, to output the resulting clock signal at an output end thereof (Fig. 11, element variable delay that does the phase shifting);

AAPA does not disclose a discriminator circuit that has the data signal as its input.

In the same field of endeavor, however, Miyashita discloses said discriminator circuit is supplied with said received data signal at a data input end thereof to discriminate said received data signal based on a clock signal for discrimination supplied to a clock input

terminal thereof to output a data signal at an output end thereof (Fig. 7, elements 21A and 22A; wherein element 21A, 21B are interpreted as the discriminator circuit and element 22A does the phase comparison between the input signal and the discriminator output);

said second phase detector circuit compares the phase of the data signal supplied to a first input end thereof from said discriminator circuit with that of said received data signal supplied to a second input end thereof to output a comparison result at an output end thereof (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the phase discriminator, as taught by Miyashita, in the system of AAPA because this would for allow for the output data to be locked to the input data signal.

Regarding claim 24, AAPA discloses clock recovery circuit comprises:

a voltage-controlled oscillator circuit for outputting a clock signal included in said first feedback loop (Fig. 11, element VCO), the oscillation frequency of said voltage-controlled oscillator circuit is variably controlled base on an input control signal obtained by integrated output of said first phase detector (Fig. 11, element low pass filter controls the VCO in the upper path);

and a phase shift circuit included in said second feedback loop, said phase shift circuit receiving the clock signal output from said voltage-controlled oscillator circuit and an integrated output of said second integrator circuit, for shifting the phase of said clock signal in accordance with the integrated output received, to output the resulting clock signal for supply to said discriminator circuit (Fig. 11, element variable delay that does the phase shifting).

Regarding claim 15, AAPA discloses a clock and data recovery circuit (Applicant's Fig. 11) comprising:

a first feedback loop including a first phase detector circuit for detecting the phase difference between an input reference clock signal and a recovered clock signal (Fig. 11; Specification [0021]; wherein the 1st feedback loop is formed by elements 902, low pass filter, oscillator 909; the oscillation frequency being controlled by the output of the loop filter and the phase detector receives as inputs the Data input signal and VCO output. The input reference signal is the data signal and the recovered clock signal is the output of the VCO);

and a second feedback loop including a second phase detector circuit for detecting the phase difference between the data signal discriminated and output by said discriminator circuit and said received data signal (Fig. 11, elements formed by 910, low pass filter, 912);

a clock for discrimination of said discriminator circuit being supplied from a clock recovery circuit controlled by said first and second feedback loops (Fig. 11, 1st and 2nd loops giving output "Clock Out").

AAPA does not disclose a discriminator circuit that has the data signal as its input.

In the same field of endeavor, however, Miyashita discloses a discriminator circuit supplied with said received data signal (Fig. 7, elements 21A and 22A; wherein element 21A, 21B are interpreted as the discriminator circuit and element 22A does the phase comparison between the input signal and the discriminator output) and the clock signal output from said clock recovery circuit being supplied as a clock signal for discrimination by said discriminator circuit (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the phase discriminator, as taught by Miyashita, in the system of AAPA because this would for allow for the output data to be locked to the input data signal.

Regarding claim 16, AAPA discloses first feedback loop includes:

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage (Fig. 11, element 909 which receives control voltage from the loop filter output);

a first phase detector circuit receiving the clock signal output from said voltage-controlled oscillator circuit and said reference clock signal to detect the phase difference there between (Fig. 11, element 902);

and a first integrator circuit for integrating an output of said first phase detector circuit to supply the resulting output voltage to said voltage-controlled oscillator circuit as a control signal voltage (Fig. 11, element low pass filter in upper path);

and wherein said second feedback loop includes:

a second integrator circuit for integrating an output of said second phase detector circuit (Fig. 11,element low pass filter in lower feedback loop);

and a phase shift circuit supplied with said clock signal output from said voltage-controlled oscillator circuit and with an integrated output of said second integrator circuit to phase-shift the input clock signal depending on the input integrated output (Fig.11, element variable delay that does the phase shifting).

AAPA does not disclose a discriminator circuit that has the data signal as its input.

In the same field of endeavor, however, Miyashita discloses a discriminator circuit supplied with said received data signal (Fig. 7, elements 21A and 22A; wherein element 21A, 21B are interpreted as the discriminator circuit and element 22A does the phase comparison between the input signal and the discriminator output);

a second phase detector circuit supplied with the data signal output from said discriminator circuit and with said received data signal to detect the phase difference between the two signals supplied (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B);

the clock signal, output from said phase shift circuit, being supplied to said discriminator circuit as the clock for discrimination, and being output as an output clock signal (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the phase discriminator, as taught by Miyashita, in the system of AAPA because this would for allow for the output data to be locked to the input data signal.

Regarding claim 25, AAPA discloses clock recovery circuit comprises:

a voltage-controlled oscillator circuit for outputting a clock signal included in said first feedback loop (Fig. 11, element VCO), the oscillation frequency of said voltage-controlled oscillator circuit is variably controlled base on an input control signal obtained by integrated output of said first phase detector (Fig. 11, element low pass filter controls the VCO in the upper path);

and a phase shift circuit included in said second feedback loop, said phase shift circuit receiving the clock signal output from said voltage-controlled oscillator circuit and an

integrated output of said second integrator circuit, for shifting the phase of said clock signal in accordance with the integrated output received, to output the resulting clock signal for supply to said discriminator circuit (Fig. 11, element variable delay that does the phase shifting).

7. Claims 19 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter AAPA) in view of Miyashita et al (US 5610954) as applied to claims 12 – 16, 24 - 26 above, and further in view of Yonekura et al (US 5,761,617).

Regarding claim 19, AAPA does not disclose the time constant of said first feedback loop is selected to be larger than the time constant of said second feedback loop.

In the same field of endeavor, however, Yonekura discloses the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit (Abstract; column 4, lines 1- 20).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use different time constants, as taught by Yonekura, in the system of AAPA because this would allow for different rates of convergence of the loops.

Regarding claim 21, AAPA does not disclose the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit.

In the same field of endeavor, however, Yonekura discloses the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit (Abstract; column 4, lines 1- 20).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use different time constants, as taught by Yonekura, in the system of AAPA because this would allow for different rates of convergence of the loops.

Claim 20 recites the same limitation as claim 19 and is therefore similarly rejected as claim 19.

Claim 22 recites the same limitation as claim 21 and is therefore similarly rejected as claim 21.

8. Claims 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter AAPA) in view of Miyashita et al (US 5610954) as applied to claim 14 above, and further in view of Anumula et al (US 6,566,967).

Regarding claim 17, AAPA does not disclose a selection circuit for selecting said received data signal or said reference clock signal.

In the same field of endeavor, however, Anumula discloses said first phase detector circuit includes a selection circuit for selecting said received data signal or said reference clock signal, as a signal to be subjected to phase comparison with said clock

signal (Fig 2, element 220B, 206; column 3, lines 53 – 55; wherein the selector is element 220B and the phase detector is element 206).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the selector, as taught by Anumula, in the system of AAPA because this would allow for different inputs to be locked onto.

Regarding claim 18, AAPA discloses first feedback loop includes:

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage (Fig. 11, element 909 which receives control voltage from the loop filter output);

a first phase detector circuit supplied with a clock signal output from said voltage-controlled oscillator circuit and with a signal from said selection circuit to detect the phase difference therebetween (Fig. 11, element 902);

and a first integrator circuit for integrating an output of said first phase detector circuit to supply the resulting output voltage as a control signal voltage to said voltage-controlled oscillator circuit (Fig. 11, element low pass filter in upper path);

and wherein said second feedback loop includes:

a second integrator circuit for integrating an output of said second phase detector circuit; and a phase shift circuit supplied with a clock signal output from said voltage-controlled oscillator circuit (Fig. 11,element low pass filter in lower feedback loop) and

with an integrated output of said second integrator circuit to shift the phase of the input clock signal in accordance with said integrated output supplied to output the resulting clock signal (Fig.11, element variable delay that does the phase shifting);

AAPA does not disclose a discriminator circuit that has the data signal as its input.

In the same field of endeavor, however, Miyashita discloses a discriminator circuit supplied with said received data signal (Fig. 7, elements 21A and 22A; wherein element 21A, 21B are interpreted as the discriminator circuit and element 22A does the phase comparison between the input signal and the discriminator output);

a second phase detector circuit supplied with an output of said discriminator circuit and with said received data signal to detect the phase difference there between (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B);

the clock signal output from said phase shift circuit being supplied to said discriminator circuit as a signal for discrimination and being output as an output clock signal (Fig. 7, element 21B which receives a delayed signal from the flip-flop 21A and feeds it to the other discriminator 21B).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the phase discriminator, as taught by Miyashita, in the system of AAPA because this would for allow for the output data to be locked to the input data signal.

In the same field of endeavor, however, Anumula discloses a selection circuit supplied with a reference clock signal and with said received data signal to output one of the signals based on a selection control signal (Fig 2, element 220B, 206; column 3, lines 53 – 55; wherein the selector is element 220B and the phase detector is element 206).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the selector, as taught by Anumula, in the system of AAPA because this would allow for different inputs to be locked onto.

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter AAPA), Miyashita et al (US 5610954) and Anumula et al (US 6,566,967) as applied to claim 18 above, and further in view of Yonekura et al (US 5,761,617).

Regarding claim 23, AAPA does not disclose the time constant of said first feedback loop is selected to be larger than the time constant of said second feedback loop.

In the same field of endeavor, however, Yonekura discloses the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit (Abstract; column 4, lines 1- 20).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use different time constants, as taught by Yonekura, in the

system of AAPA because this would allow for different rates of convergence of the loops.

Other Prior Art Cited

10. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to PLLs:

Larsson (US 6,310,498) discloses digital phase selection circuitry and method for reducing jitter.

Lysdal et al. (US 6,438,178) discloses an integrated circuit for receiving a data stream that uses a PLL.

Harrison (US 6,680,874) discloses delay lock loop circuit useful in a synchronous system and associated methods.

Hansson (US 6,956,921) discloses clock and data recovery circuit.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADOLF DSOUZA whose telephone number is (571)272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID PAYNE can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611